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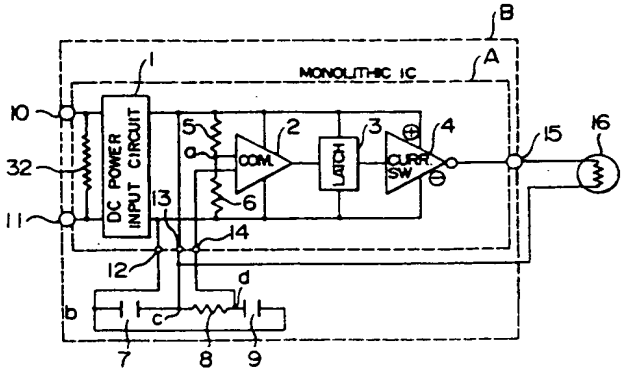
(54) Electronic delay detonator.

(57) An electronic delay detonator for igniting an ignition resistor a predetermined delay time after supply of electric power from a blasting machine comprises two input terminals (10, 11) for receiving the electric power supplied from the blasting machine, a diode-bridge circuit (D_1–D_4) connected to the input terminals, a power supply capacitor (7) connected to the output of the diode-bridge circuit, an RC charging circuit (8, 9) connected in parallel with the capacitor and having a predetermined time constant, and a monolithic IC. The monolithic IC includes a reference generation circuit (5, 6) for generating a compare reference voltage by dividing the power supply by dividing resistors, a voltage comparator (2) for comparing the voltage charged in the capacitor of the charging circuit with the compare reference voltage, a signal latch circuit (3) for holding the output of the comparator and a transistor current switching circuit (4) responsive to the output of the signal latch circuit to for supplying the electric energy of the power supply capacitor to the ignition resistor of the detonator. The overall circuit is in a hybrid IC module. A resistor (32) having a constant resistance sufficiently distinguishable from an internal resistance of the detonator is connected across the two input terminals to bypass a stray current and enable checking of connection continuity of series-connected detonators.



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ELECTRONIC DELAY DETONATOR

BACKGROUND OF THE INVENTION

The present invention relates to an electric detonator having an electronic delay ignitor, and more particularly to a hybrid IC ignition circuit to be packaged in an electric detonator.

Prior art electric detonators having electronic delay ignitors are disclosed in U.S. Patent 4,311,096, U.S. Patent 4,445,435, U.S. Patent 4,586,437 issued on May 6, 1986 and owned by the present assignee and Japanese Patent Application Laid-Open No. 57-142496 laid open on September 3, 1982 and invented by two of the present inventors. The detonator is intended to initiate explosion of explosives such as dynamite or water gel explosive. Those are electric detonators each having an electronic ignition circuit including an energy storing capacitor, an electronic delay circuit and a switching element. The detonator is ignited by supplying an energy stored in the capacitor to a detonator ignition resistor through the switching element a predetermined time after discharging of a blasting machine.

In the detonator which uses analog delay means comprising a capacitor C and a resistor R as disclosed in U.S. Patent 4,311,096 and Japanese Patent Application Laid-Open No. 57-142496, a time precision is significantly influenced by an applied voltage, a temperature change and

variance in individual components and hence it has a problem in practical use. The time precision or delay accuracy of such detonator is not much different than that of a prior art delay powder type electric detonator.

When the analog delay switching circuit having a capacitor (C) 9 and a resistor (R) 8 shown in Fig. 6 is implemented by a monolithic IC, it is difficult in manufacture to integrate a switching thyristor (SCR) 19 and a PUT (programmable unijunction transistor) 18 having reference voltage resistors 5 and 6 connected thereto into the monolithic IC. Even if they are integrated, a power supply capacitor 7 must be large because of an insufficient delay accuracy and a large current consumption. Accordingly, it is not appropriate to the IC delay element of the electric detonator.

In addition, since the electronic delay detonator contains the energy storing capacitor 7, if input terminals 10 and 11 are opened, an external stray current is gradually stored in the energy storing capacitor 7 through an input line.

As the amount of stored energy increases, the stored energy activates the delay switching circuit so that a trigger signal is applied to the switching element 19 such as a thyristor and the ignition electric energy stored in the capacitor 7 flow into an ignition resistor wire 16 through the switching element 19 to heat the resistor wire 16. As a result, the detonator is ignited inadvertently.

The amount of stored energy depends on whether the stray current is pulsive (single pulse or repetitive pulse) or continuous. When the stray current is continuous, the electronic delay detonator is fired in several seconds to several tens seconds when the stray current is approximately 2 mA at 10 volts. Further, in those electronic delay detonators, inconveniently it is not possible to check and measure continuity and series-connection resistance. The problems in the stray current and continuity check of the detonator also apply to digital delay means to be described below.

The detonator having digital delay means as disclosed in U.S. Patents 4,445,435 and 4,586,437 has a higher time precision than that of the analog delay switching circuit but it is not practical to use in a disposable detonator because it must use an expensive quartz resonator or ceramic resonator. If a relatively inexpensive CR oscillator is used, an oscillation IC and a counter IC are required and a separate current switching element (for example SCR) must be provided, as a result, it is difficult to integrate those element in one chip and size reduction is restricted.

SUMMARY OF THE INVENTION

It is an object of the present invention to provide a compact, low cost and highly reliable electronic delay detonator which consumes low power and is suitable for disposable use.

It is another object of the present invention to provide an electronic delay detonator which prevents malfunction due to a stray current.

It is a further object of the present invention to provide an electronic delay detonator of a configuration in which proper electrical connection and the number of connections of plural detonators can be readily checked by electrical means significantly in a blasting work using a large number of detonators.

In order to achieve the above objects, in accordance with the present invention, there is provided an electronic delay detonator having an electronic delay timer switch comprising a power supply circuit, an electrical energy storing capacitor (power supply capacitor) for a timer and ignition, a CR charging circuit which functions as a delay element and has an output of the power input circuit applied thereto, a compare reference voltage generating circuit which divides the output of the power supply circuit by a ratio of resistors, a voltage comparator which compares a voltage stored in a capacitor of the CR charging circuit with the compare reference voltage, a signal latch circuit, and a detonator ignition current switching circuit which is activated by an output of the signal latch circuit. The latch circuit may be dispensed with by bearing a latch function to the voltage comparator or the current switching circuit. The power supply circuit, the compare reference voltage generating circuit, the latch circuit and the switching circuit are integrated into a monolithic

IC and the entire assembly is assembled into a hybrid IC.

In accordance with one feature of the electronic delay detonator of the present invention, the monolithic IC of the electronic ignition timer switch includes the power input circuit, the compare reference voltage generating circuit, the voltage comparator, the latch circuit and the switching circuit. It may be possible to integrate those circuits and the CR charging circuit into the monolithic IC for a limited short time setting, it is preferable to arrange the CR charging circuit externally of the monolithic IC in order to obtain a practical delay time ($\sim$ 8 seconds) of the electronic delay detonator and allow setting of any desired delay time. If the IC which integrates the power supply circuit therein is difficult to attain, the power supply circuit may be arranged externally to form a hybrid IC.

Due to use of the power supply capacitor of an appropriate diameter (about 6 mm to 10 mm) to the detonator, the monolithic IC which includes the compare reference voltage generating circuit, the voltage comparator, the latch circuit and the switching circuit must meet electrical characteristics of input voltage; lower than 20 V, circuit consumption current when the switch is off; lower than 700 - 800 mA (a long-time timer is attained by suppressing the circuit consumption current), a switching circuit saturation voltage; lower than 2 V (when output current is 1A), and a maximum allowable output current; 10A. Thus, a voltage drop during the circuit operation is suppressed,

the use of a small diameter capacitor (small capacity capacitor) is permitted, and the electronic delay detonator having suitable shape and size (e.g. a diameter of about 6 to 10 mm and a length of lower than 100 mm) to the ignition is provided.

When the input voltage is lower than 20 V and the time precision of the detonator is to be less than 0.1% with the exception of variation of the individual elements, it is preferable that the sensitivity of the voltage comparator is larger than 12 mV, an offset voltage is less than several mV and an input impedance is higher than 100 MΩ.

The present detonator with the electronic timer switch can be readily constricted by separately manufacturing the electronic timer switch and connecting it to a leg wire of a conventional detonator.

In accordance with another feature of the present invention, resistor means is connected to an input terminal of the electronic delay detonator in parallel with the power supply capacitor of the detonator to bypass a stray current thereto.

For the electronic delay detonator of the present invention, various tests were made for the stray current and it was found that the electronic delay detonator is not ignited if the resistance of the resistor means is substantially 10 - 500 Ω for a continuous stray current of a low current (lower than 0.3 A) and a low voltage (lower than 20 V). In order to allow connection-continuity check

and counting of the number of connected detonators effectively, it is preferable that the resistance is selected between 100 - 200 Ω.

BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 is a block diagram of a circuit of an embodiment of an electronic delay detonator of the present invention,

Fig. 2 is a block diagram of blasting circuit connection of a plurality of electronic delay detonators in accordance with another embodiment of the present invention,

Fig. 3 is a circuit diagram of a monolithic IC in accordance with an embodiment of the present invention,

Fig. 4A to 4C are views of front surface, rear surface and longitudinal section, taken along a line 4C - 4C, respectively, of a hybrid circuit board of an electronic ignition circuit for the detonator of the present invention,

Fig. 5 is a longitudinal sectional view of an overall detonator in accordance with an embodiment of the present invention, and

Fig. 6 is a circuit diagram of a prior art analog delay detonator. Here, like reference numerals and characters indicate like parts in the drawings.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

Fig. 1 show a block diagram of an electronic timer switch in accordance with one embodiment of the present

invention.

A chain line block A is a circuit in a monolithic IC structure (semiconductor chip). A size of the semiconductor chip is approximately 2 mm square. A block B is a substrate made of glass epoxy or ceramic, or a film carrier wiring portion. The semiconductor chip of the block A comprises a power input circuit 1 usually formed of a diode bridge, a voltage comparator 2, a latch circuit 3, a detonator ignition current switching circuit 4, a voltage divider including series-connected resistors 5 and 6 for generating a compare reference voltage, power supply terminals 10 and 11 adapted to connect to a blasting machine, negative and positive DC power supply terminals 12 and 13, a voltage comparator input terminal 14 and a switch output terminal 15 for establishing a current path for an ignition resistor 16 made of e.g. platinum wire.

The substrate B comprises, as off-chip elements of the IC chip A, a capacitor (power supply capacitor) 7 for storing electrical energy for timer operation and igniting and a resistor 8 and a capacitor 9 which form a delay time constant circuit.

Configuration and function of the IC chip are explained by an equivalent circuit. The power input circuit (which is powered by a D.C. power from the blasting machine to form a unidirectional circuit is practically essential as disclosed in U.S. Patent 4,586,437 of the present assignee and it is a DC power supply rectification and supply circuit by which power lines from the blasting

machine may be connected with the input terminals freely regardless of polarity. In the equivalent circuit, rectifier elements each having a current of 0.5 A - 1 A are configured into a bridge rectifier circuit or a half wave rectifier circuit. Essentially, a resistor 32 for bypassing the stray current is connected across the input terminals 10 and 11.

The DC output terminals of the power input circuit 1 are connected to the positive (+) power supply terminal 13 and the negative (-) power supply terminal 12, and the junction a of the dividing resistors 5 and 6 (having a resistance of 30 - 100 kΩ) and the voltage comparator input terminal 14 are connected to the respective input terminals of the IC analog voltage comparator 2 of a differential amplifier configuration (having a differential input voltage sensitivity of 3 mV).

The output of the comparator 2 is supplied to the signal latch circuit 3 and the output of the signal latch circuit 3 is supplied to the detonator ignition current switching circuit 4 (peak current : 5.0 A and maximum limit: 10A). The signal latch circuit 3 latches the signal from the voltage comparator 2 so that it sends out a stable signal to the switching circuit 4. If the signal latch function is included in the IC analog voltage comparator 2 or the detonator ignition current switching circuit 4, the signal latch circuit 3 may be omitted.

The detonator ignition current switching circuit 4 establishes a conduction path between the output terminal

15 and the (-) power supply terminal 13, and hence, permits establishment of an igniting discharge path including the above conduction path, the capacitor 7 and an ignition resistor 16.

The power input capacitor 7 (electrolytic capacitor : 300 μF) is connected off the IC chip to the output terminal of the power input circuit 1, and the time setting resistor 8 (metalic or carbon film resistor : several tens kΩ to 10 MΩ) and the capacitor 9 (chip capacitor : 0.001 - 10 μF) are connected in series to the output terminal of the power input circuit. A junction b is connected to the negative (-) DC power supply terminal 10, a junction c is connected to the positive (+) DC power supply terminal 13, and a junction d is connected to the voltage comparator input terminal 14.

The discharge current of the power supply capacitor 7 is supplied up to 10 A in a short time period such as less than a few milliseconds, as the timer switch output ignition current, from the t power supply terminal 13 to the ignition resistor 16 of the electric detonator through the output terminal 15, to ignite the electric detonator.

When a voltage of approximately 15 V per detonator is applied for several ms from an external electrical blasting machine through the power supply input terminals 10 and 11, the + voltage is always applied to the + power supply terminal 13 and the - voltage is always supplied to the - power supply terminal 12 by the power input circuit 1 of the diode bridge configuration, and the + voltage is

applied to the junction c of the power supply capacitor 7 and the resistor 8 and the - voltage is applied to the junction b of the power supply capacitor 7 and the capacitor 9. As a result, the necessary voltage (approximately 10 V) is stored in the power supply capacitor 7. In this manner, the power supply capacitor 7 stores the energy necessary to the operation of the timer and the energy necessary to ignite the detonator, to a rated voltage.

When a high precision electronic timer is desired, a resistor and a zener diode may be connected to the output of the power input circuit 1 to impart a constant voltage characteristic, as disclosed in the U.S. Patent 4,586,437.

As the power supply capacitor 7 is charged, the capacitor 9 is charged through the resistor 8 by a time constant determined by a product of the capacitance of the capacitor 9 and the resistance of the resistor 8, for example, by a time constant of 10 - several hundreds ms. The voltage at the junction a of the resistors 5 and 6 and the voltage stored in the capacitor 9 are supplied to respective input terminals of the IC analog voltage comparator 2.

In order that a long delay time may be set in a substantially linear charge time-charge voltage characteristic of the time constant circuit 8 and 9, the resistance ratio of the voltage divider resistors 5 and 6 is set to generate a compare reference voltage which is equivalent to a terminal voltage of the time constant circuit 8 and 9 at 1.1 times its time constant after the beginning of

charging. For example, the resistance ratio of resistors 5 and 6 may be set at 1 : 2 and the compare reference voltage applied to the comparator 2 may be set preferably at 2/3 of the power supply voltage.

The power is supplied to the power supply input terminals 10 and 11 to charge the capacitor 9, and a predetermined delay time (10 - several hundreds ms) after the initiation of the supply of power from the blasting machine, the voltage across the capacitor 9 is approximately 3 mV larger than the divided voltage at the junction a of the resistors 5 and 6, and the IC analog voltage comparator 2 produces a voltage signal corresponding to the power supply voltage (approximately equal to the voltage e.g. approximately 10 V stored in the power supply capacitor 7), and it is latched in the signal latch circuit 3. As the signal corresponding to the power supply voltage is latched, the signal latch circuit 3 also produces a voltage approximately equal to the voltage of the power supply capacitor 7 (approximately 10 V), and it is supplied to the detonator ignition current switching circuit 4 to turn on the current switching circuit 4 so that a conduction path is established between the output terminal 15 and the (-) power supply terminal 12. As a result, the charge stored in the power supply capacitor 7 flows through the detonator ignition resistor 16 connected externaly between the (+) power supply terminal 13 and the output terminal 15, up to 5 A for 0.5 - several ms. The detonator ignition resistor 16 is thus ignited with a preset delay time (10 - several

hundreds ms) after discharging of the blasting machine. Namely, the setting time t of the present electronic timer switch is determined by the time constant of the resistor 8 (R) and the capacitor 9 (C) stated above.

Fig. 2 shows an embodiment of the present invention in which a plurality of detonators essentially shown in Fig. 1 are serially connected to the blasting machine. Numerals 30_1, 30_2, ... 30_n denote the detonator ignition circuit blocks, numeral 31 denotes a blasting machine with a fire switch 33 which is usually a variable high voltage supply, and numerals 32_1, 32_2, ... 32_n denote stray current bypassing resistors connected across the input terminals 10 and 11.

For example, the energy storing capacitor 7 is an aluminum electrolytic capacitor of 330 μF, the delay capacitor 9 is 0.1 μF. The delay resistor 8 is selected to be 100 kΩ based on a predetermined delay time and the bypassing resistor 32 is 20 Ω.

A D.C. continuous current of 0.3 A was supplied to the input terminals 10 and 11 of the electronic delay detonator as the stray current, but the detonator was not ignited. On the other hand, in the electronic delay detonator in which the stray current bypassing resistor 32 was eliminated in the circuit of Fig. 2, the detonator was ignited in 2 - 3 seconds under the same condition of the stray current.

In the connection circuit of Fig. 2, the detonator ignition circuits 30_1, 30_2, ... 30_n are sequentially ignited

after the predetermined delay time at a selected time interval between 10 - 30 ms. As a result, ground vibration adversely affecting in a periphery of the blasting point is substantially released. On the basis of the inventors' finding on vibration reduction, the constants of the delay time constant circuits of the ignition circuits are changed by a predetermined increment at a high precision. The resistor 8 and the capacitor 9 of the time constant circuit are preferably arranged off the chip to allow, the use and adjustment of different time constants. The substantial time constant adjustment is usually made by selecting the values of the resistor 8 and the capacitor 9 and the fine adjustment is made by trimming the resistor 8.

In the blasting machine circuit of Fig. 2, the number of detonators connected can be counted by providing a conventionally known counter-type (digital) resistance measurement circuit and converting a total resistance of the circuit to the number of electric detonators. For example, if the resistance of the input terminal bypassing resistor 32 is 100 Ω and 50 detonators are connected in series, the total resistance is equal to 5 kΩ plus a bus (leading wire) resistance. The internal resistance of the prior art electric detonator is approximately 1 Ω, but, the values for detonator are largely uneven due to environmental temperature characteristics and fabrication factors of ignition resistor (platinum wire). Therefore, it has been difficult to determine the number of connected detonators by

measuring the total resistance by the number of detonators. By providing a resistor of a large constant resistance in the preceding stage of diode-bridge power input circuit of each detonator, the number of connected detonators can be readily determined by measuring the total resistance of the connected detonators since the unevenness of ignition resistances and bus resistance are negligible.

Fig. 3 shows an embodiment of the block C of the monolithic IC of Fig. 2. Numerals 41 - 51 denote PNP or NPN transistors, numeral 52 denotes a diode, R_3 - R_{14} denote resistors, numerals 12 and 13 denote a pair of power supply terminals, numeral 14 denotes a compare input terminal, and numeral 15 denotes an ignition resistance connection terminal. The comparator 2 comprises the differentially connected transistors 41 and 42, diode-connected transistor 51 and the load transistor 43, and the latch circuit 3 comprises the PNP transistors 44 and 45, the signal holding NPN transistor 46, the diode 52 and the output NPN transistor 47. The transistor current switching circuit 4 comprises the input PNP transistor 48, the drive/conduction compensation NPN transistor 49 and the switching NPN transistor 50 for energizing the ignition resistor 16.

Fig. 4A - 4C show a hybrid configuration (module) of the detonator ignition circuit where the diode-bridge power input circuit 1 and bypass resistor 32 are made in the form of discrete component, as shown in the embodiment of Fig. 2.

Fig. 5 shows an overall view of the electric detonator in accordance with the present invention. Numeral 7 denotes a power electrolytic capacitor, numerals 10' and 11' denote leg wires for lead-out from input terminals 10 and 11, numeral 20 denotes a plug a plastic cap, numeral 21 denotes a plastic casing , numeral 22 denotes a plastic plug, numeral 23 denotes an ignition agent plastic cup, numeral 24 denotes an inner capsule, numeral 25 denotes a primer charge, numeral 26 denotes a base charge, numeral 27 denote a shell, numeral 16 denotes an ignition ressitor, C denotes a monolithic IC package, and B denotes a hybrid IC glass. The ignition time of the detonator with the electronic timer switch constructed in the hybrid IC as shown in Fig. 1 in accordance with the above embodiment was measured. As comparative examples, the ignition times of the electronic delay detonators of the delay powder type and the analog CR circuit type (Japanese Patent Application Laid-Open No. 57-142496) were measured, as shown in the following Table, where $\bar{X}$ indicates a median and σ indicates a variance.

Nominal Time	Conventional Electric Detonator (delay powder type)			Analog CR Delay circuit Detonator (Pat.Appln. Laid Open 57-142496)			Present Detonator		
(ms)	$\overline{X}$ (ms)	σ	$3\sigma/\overline{X}$ x100 (%)	$\overline{X}$	σ	$3\sigma/\overline{X}$ x100 (%)	$\overline{X}$	σ	$3\sigma/\overline{X}$ x100 (%)
500	560	39.6	21.2	495.6	14.3	8.7	499.4	3.1	1.8
1000	1090	48.5	13.3	992.1	13.2	4.0	999.7	3.7	1.1
5100	5085	158.4	9.3	5109.2	23.6	1.4	5100.7	8.7	0.5
7500	7762	167.6	6.4	7518.6	37.2	1.5	7500.2	20.4	0.6

(Measured at 20°C)

In accordance with the embodiment of the present invention, the compact and inexpensive detonator with the electronic timer switch having a practically long time and a high time precision is provided, which comprises the monolithic IC (for example, 2 mm square) and the off-chip power supply capacitor, time setting resistor and time setting capacitor, with the resistors being trimmed by a known automatic trimming apparatus such as an abrasive powder blaster to adjust the setting time.

In accordance with the present invention, the overall circuit of the electronic timer switch including the monolithic IC, the power supply capacitor, the time constant resistor and the time constant capacitor can be formed by a film carrier or glass epoxy or ceramic substrate. Thus, the manufacturing process can be significantly simplified and automated.

The present invention can provide the detonator with the electronic timer which is of practicable cost and construction.

The above timer circuit of IC configuration may be modified by using a bipolar-MOS (transistor) technologies.

CLAIMS:

1. An electronic delay detonator for driving an ignition device a predetermined delay time after supply of electrical energy, comprising: in a hybrid IC configuration,

input terminal means (10, 11) for supplying the electrical energy to said electronic delay detonator;

a first capacitor (7) for storing the electrical energy;

release prevention means (1) connected between said input terminal means and said first capacitor for preventing the electrical energy stored through said input terminal means from being released;

a time constant circuit (8, 9) connected in parallel with said first capacitor and including a second capacitor (9) and a first resistor (8) for charging electrical power supplied from said input terminal means at a time constant corresponding to said predetermined delay time and determined by the product of a capacitance of said second capacitor and a resistance of said first resistor;

a reference voltage generation circuit (5, 6) including a voltage divider connected across said first capacitor for generating a compare reference voltage;

a voltage comparator (2) for comparing the charged voltage of said time constant circuit with the compare reference voltage of said reference voltage generating circuit to produce an output signal when the charged voltage exceeds the compare reference voltage;

and

a transistor current switching circuit (4) responsive to the output signal of said voltage comparator for establishing an electrical path to supply the electrical energy stored in said first capacitor to an ignition resistor of said ignition device.

2. An electronic delay detonator according to Claim 1 further comprising a signal latch circuit (3) connected between said voltage comparator and said current switching circuit, for latching the output of said voltage comparator to drive said current switching circuit by the latch output.

3. An electronic delay detonator according to Claim 1 further comprising a second resistor (32) connected across said input terminal means (10, 11) for preventing a stray current from flowing into said first capacitor.

4. An electronic delay detonator according to Claim 3 wherein said second resistor (32) has a constant resistance sufficiently distinguishable from an internal resistance of the electric circuit of said electronic delay detonator.

5. An electronic delay detonator according to Claim 2 wherein at least said compare reference voltage generation circuit, said voltage comparator, said signal latch circuit and said detonator ignition current switching circuit are assembled in a monolithic bipolar integrated circuit, one end of said resistor of said ignition device is connected to a high potential side of said first

capacitor and the other end thereof is connected to a switching transistor of said current switching circuit, and said current switching circuit, when it is actuated, establishes a conductive path across said first capacitor to connect the resistor of said ignition device.

6. An electronic delay detonator according to Claim 5 comprising an elongated substrate on which said bipolar monolithic integrated circuit, said release prevention means, said first and second resistors and said second capacitor are packaged in module, and an elongated detonator casing having an inner diameter defined substantially by an outer diameter of said first capacitor, wherein a main surface of said substrate is arranged normally to one end surface of said first capacitor to extend therefrom longitudinally of said casing, and dimensions of a cross section of said module are defined to be no larger than the area of said one end surface of the first capacitor.

7. An electronic delay detonator according to Claim 5 wherein said monolithic bipolar integrated circuit has first and second power supply terminals (13, 12) for receiving the electrical energy stored in said first capacitor (7) as a power source, said compare reference voltage generation circuit has third and fourth resistor (5, 6) connected in series between said first and second power supply terminals to form a voltage divider, said voltage comparator has first and second transistors (41, 42) of a first conductivity type and a third load

transistor (43) of a second conductivity to form a differential amplifier, said first transistor (41) has a base electrode to receive the output of said time constant circuit (8, 9), said second transistor (42) has a base electrode connected to said third and fourth resistors of said voltage divider, said third transistor has a base electrode connected to said first power supply terminal (13), a collector electrode of said first transistor and a collector electrode of said second transistor, the output of said comparator is taken out at the junction of the collector electrodes of said first and third transistors, said signal latch circuit has fourth and fifth transistors (44, 45) of the second conductivity type having base electrodes for receiving the output of said comparator in parallel and collector electrodes connected to respective load resistors, and sixth and seventh transistors (46, 47) of the first conductivity type driven by the collector outputs of said fourth and fifth transistors and load resistors connected thereto, said sixth transistor (46) has a series circuit of the load resistor (R4, R5) and a diode (52) connected between a collector electrode and the first power supply terminal, the junction of said series circuit is connected to a base electrode of said fourth transistor (44) so that the output signal of said comparator is held as long as substantial energizing charge exists in said first capacitor to cooperate with said fourth and keep said fifth and seventh transistors conductive, said detonator ignition current switching

circuit (4) has an eighth transistor (48) of the second conductivity which conducts in response to the conduction of said seventh transistor, and ninth and tenth transistors (49, 50) of the first conductivity type having base terminals connected to a collector electrode of said eighth transistors, collectors connected to terminals connected to one end of said ignition resistor (16), and emitter electrodes connected to the second power supply terminal (12), and the emitter electrode of said ninth transistor is connected to the base electrode of said tenth transistor.

8. An electronic delay detonator according to Claim 1 wherein said first capacitor has a capacitance of several hundreds μF, said second capacitor has a capacitance of 0.001 - 10 μF, and said first resistor has a resistance of several tens kΩ - 10 MΩ.

9. An electronic delay detonator according to Claim 1 wherein said release prevention means includes a plurality of bridge-connected diodes or a plurality of doubler-connected diodes.

10. An electronic delay detonator acomprising:

first and second power input lines (10, 11);

energy storing means (7) connected to said first and second power input lines;

delay means (8, 9) connected to said first and second power input lines, for producing an output when energy stored in said energy storing means reaches a predetermined amount;

means (2 - 6) for igniting said detonator in

response to said output; and

a resistor (32) connected between said first and second power input lines.

11. An electronic delay detonator according to Claim 10 wherein said resistor is predetermined at a constant resistance of 10 Ω up to 500 Ω.

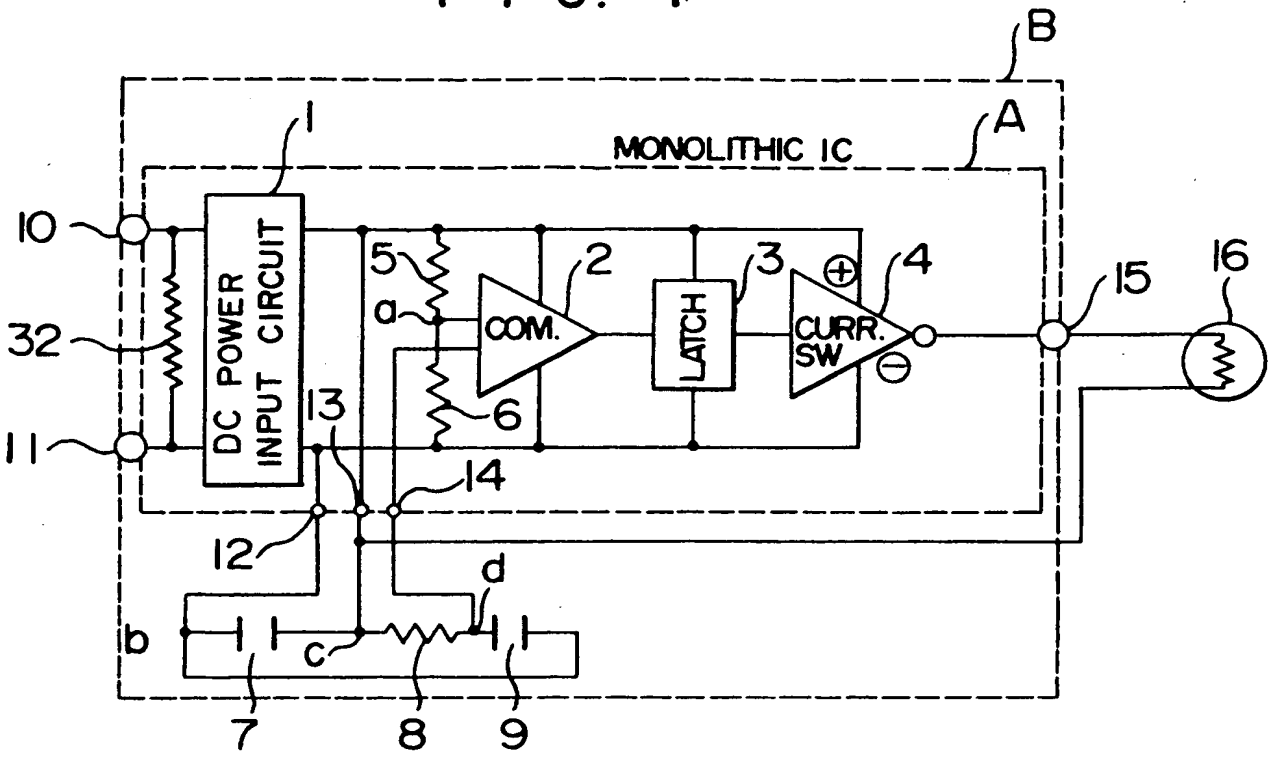
12. A method for testing connection of electronic delay detonators, comprising the steps of:

(a) providing a desired number of electronic delay detonators;

each of said electronic delay detonators comprising first and second power input lines for externally receiving electrical energy, storing means connected to said first and second power input lines for storing the electrical energy, prevention means connected between said storing means and said input lines for preventing said stored energy from being released, delay means connected to said first and second power input lines for producing an output when the energy stored in said storing means reaches a predetermined amount, switching means responsive to the output of said delay means for momentarily supplying the electrical energy of said storing means to an ignition resistor, and a bypass resistor connected between said first and second power input lines and having a predetermined constant resistance distinguishably larger than an internal resistance of the detonator switching circuit in a non-actuated state and smaller than a predetermined value; and

(b) serially connecting said first and second power input lines of said detonators so as to form a blasting detonator circuit connection, measuring a series resistance of said blasting detonator circuit connection in the non-actuated state, and determining a status of connection based on the measured resistance relative to the predetermined constant resistances of said bypass resistors.

FIG. 1


B
A
MONOLITHIC IC
1
DC POWER INPUT CIRCUIT
10
32
11
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a
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COM.
2
LATCH
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CURR. SW
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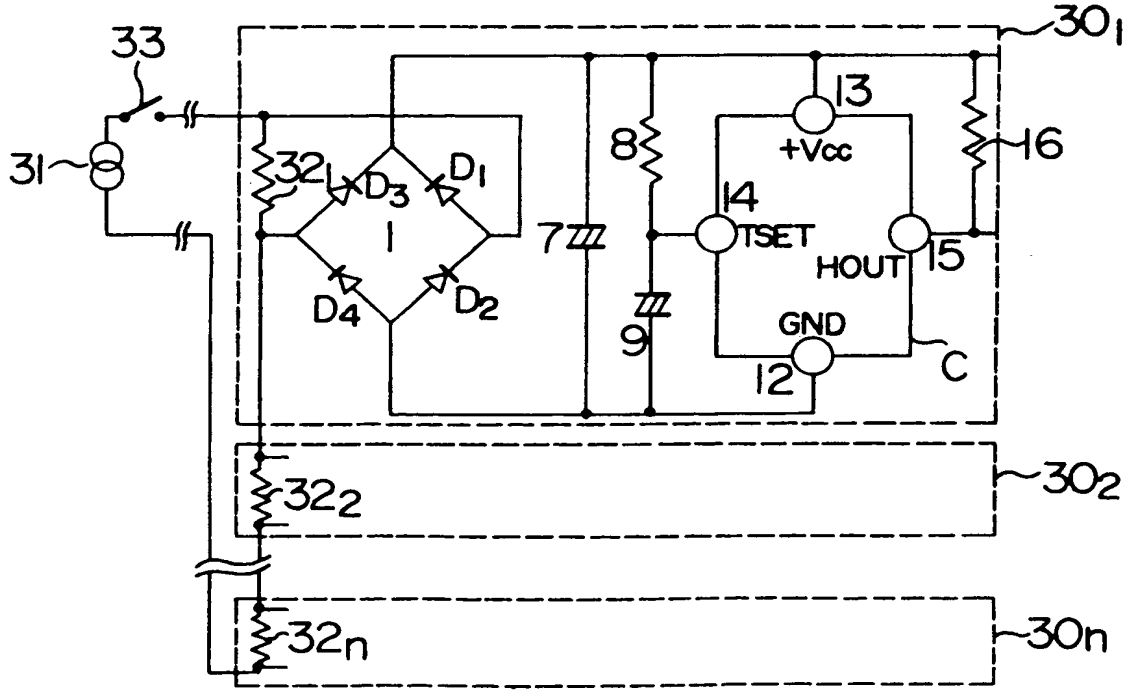
FIG. 2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C
32_2
30_2
32_n
30_n

FIG. 3

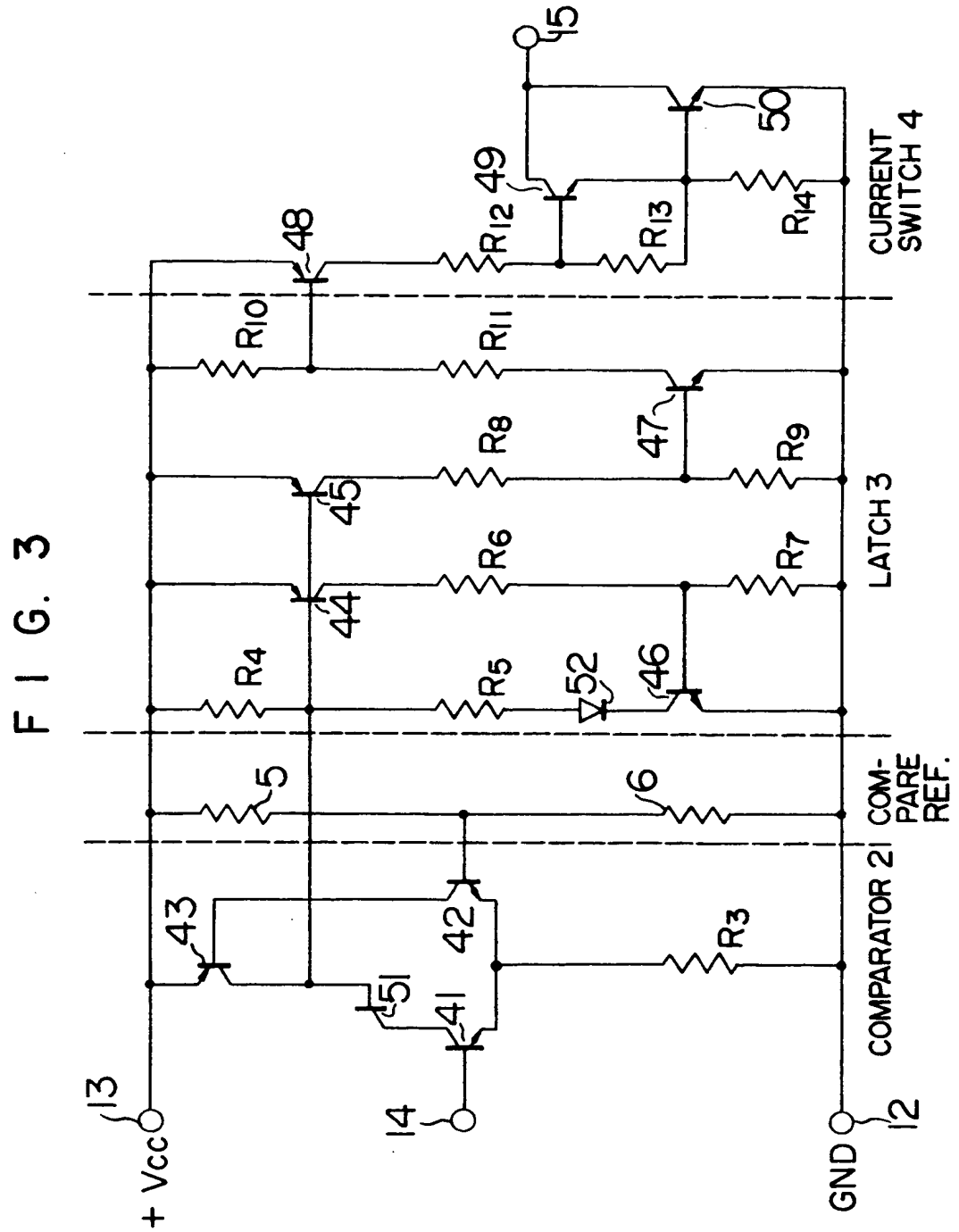

15
50
49
48
R12
R13
R14
CURRENT SWITCH 4
R10
R11
47
R8
R9
45
LATCH 3
R6
R7
44
R4
R5
52
46
5
6
COM-PARE REF.
43
42
R3
51
41
COMPARATOR 21
13
14
12
+ Vcc
GND

FIG. 4A

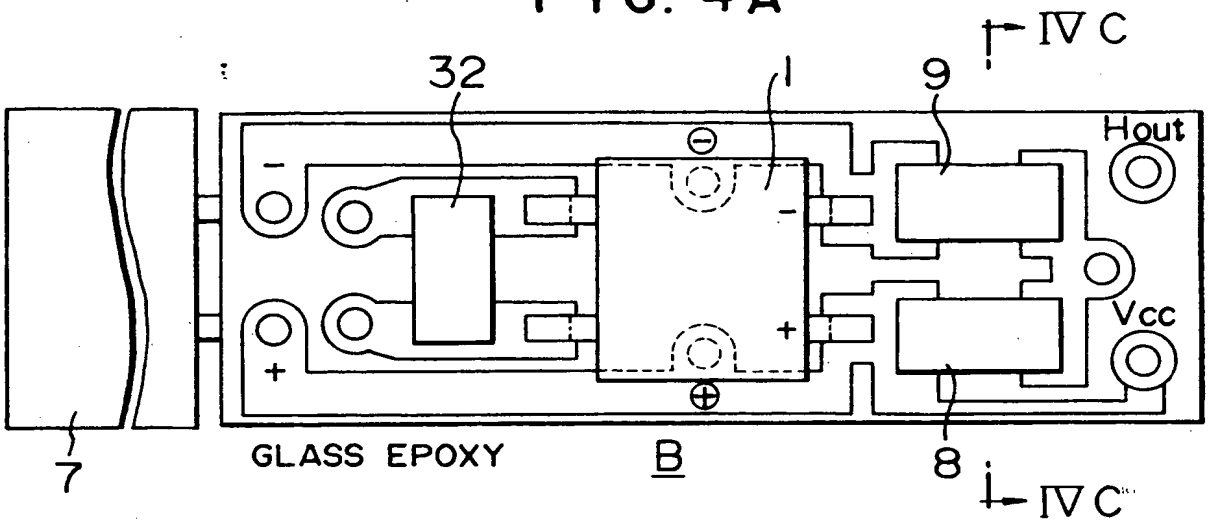


FIG. 4B

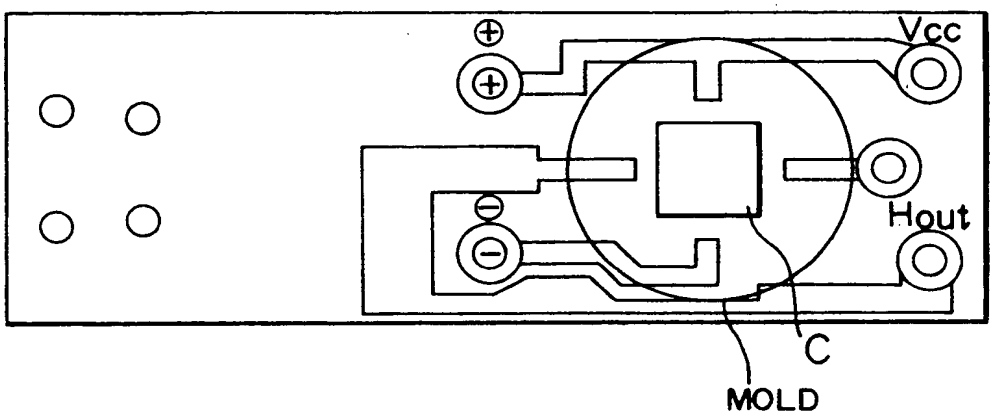


FIG. 4C

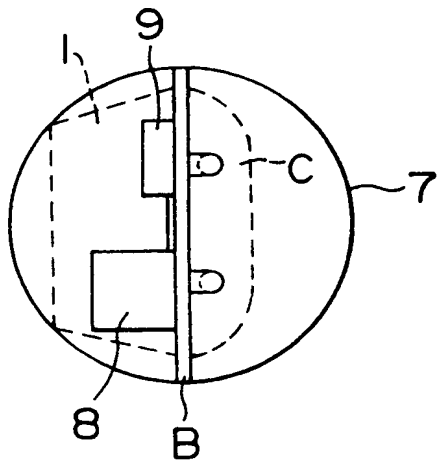


FIG. 5

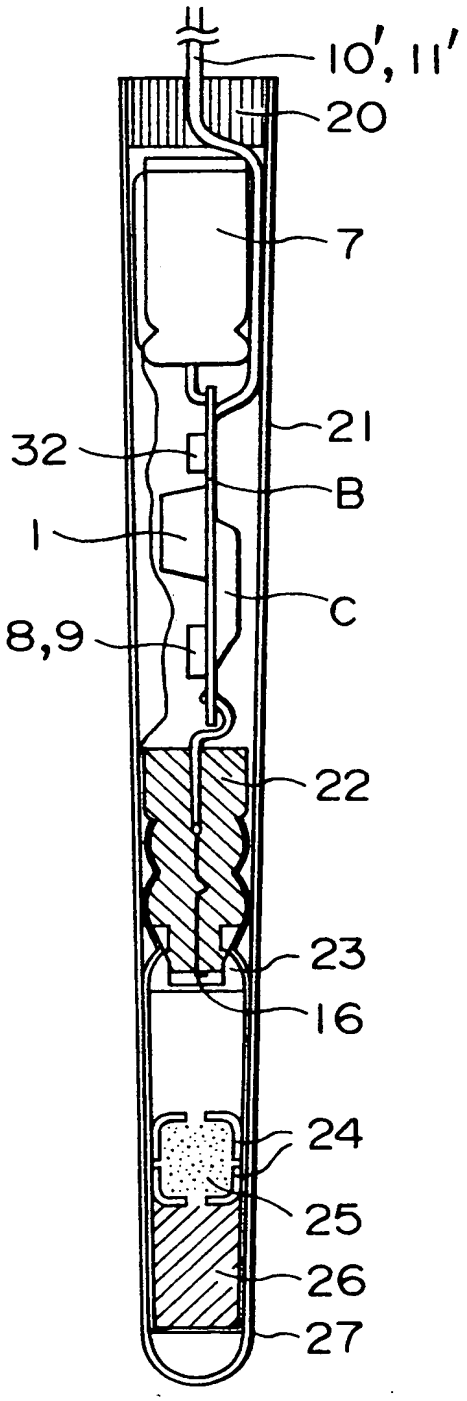
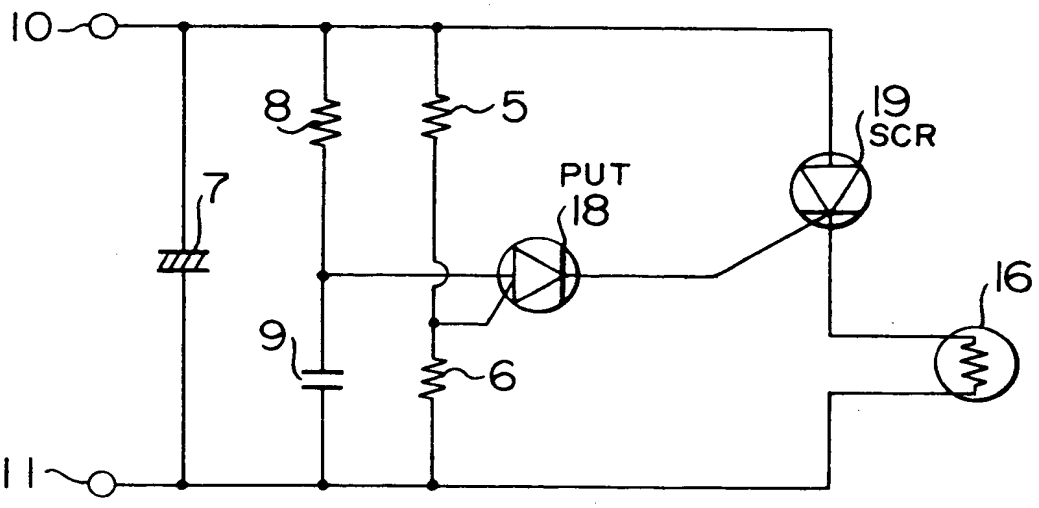


FIG. 6 PRIOR ART



European Patent Office

EUROPEAN SEARCH REPORT

0212111

Application number

EP 86107826.9

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int. Cl.4)
A	CH - A5 - 635 673 (DYNAMIT NOBEL AG) * Page 2, column 2, line 63 - page 3, column 2, line 58; page 5, column 1, line 61 - column 2, line 42; fig. 4,6 * --		F 42 C 11/06 F 42 B 3/16
A	EP - A1 - 0 093 804 ("S.A. PRB") * Totality * --		
D,A	US - A - 4 311 096 (OSWALD) * Fig. 1,5,6 * --		
D,A	US - A - 4 445 435 (OSWALD) * Totality * ----		

TECHNICAL FIELDS SEARCHED (Int. Cl.4)

F 42 C 11/00
F 42 B 3/00

The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
VIENNA	11-11-1986	KALANDRA

CATEGORY OF CITED DOCUMENTS

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